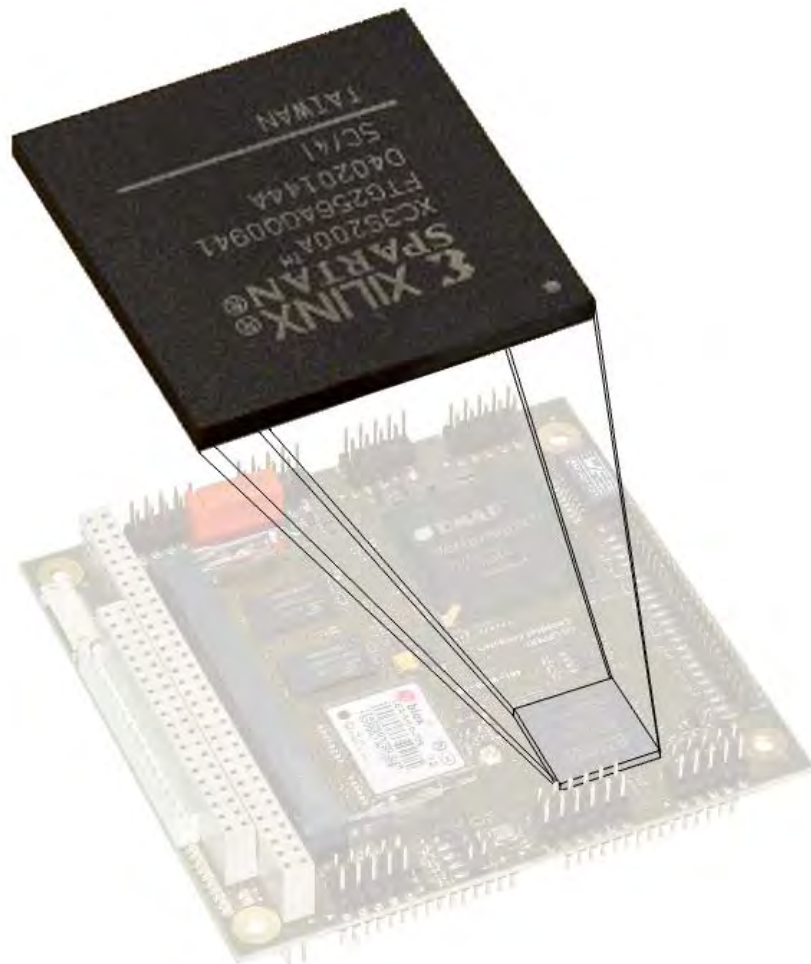


# Cool LiteRunner-86DX PC/104 CPU Board

## FPGA Manual



FME-104-CLR86DX-R0V3  
Revision 0.3 / June 11

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## *FPGA Manual Cool LiteRunner-86DX*

LiPPERT Document: FME-104-CLR86DX-R0V3 Revision 0.3

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# 1 Overview

## 1.1 Acronyms

FPGA	Field Programmable Gate Array
GPIO	General Purpose Input Output
GPS	Global Positioning System
GP-SPI	GPIO based SPI bus
LED	Light Emitting Diode
LPC	Low Pin Count bus
PWR	Power
SMB	System Management Bus
SMC	System Management Controller
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver Transmitter
SoC	System on Chip

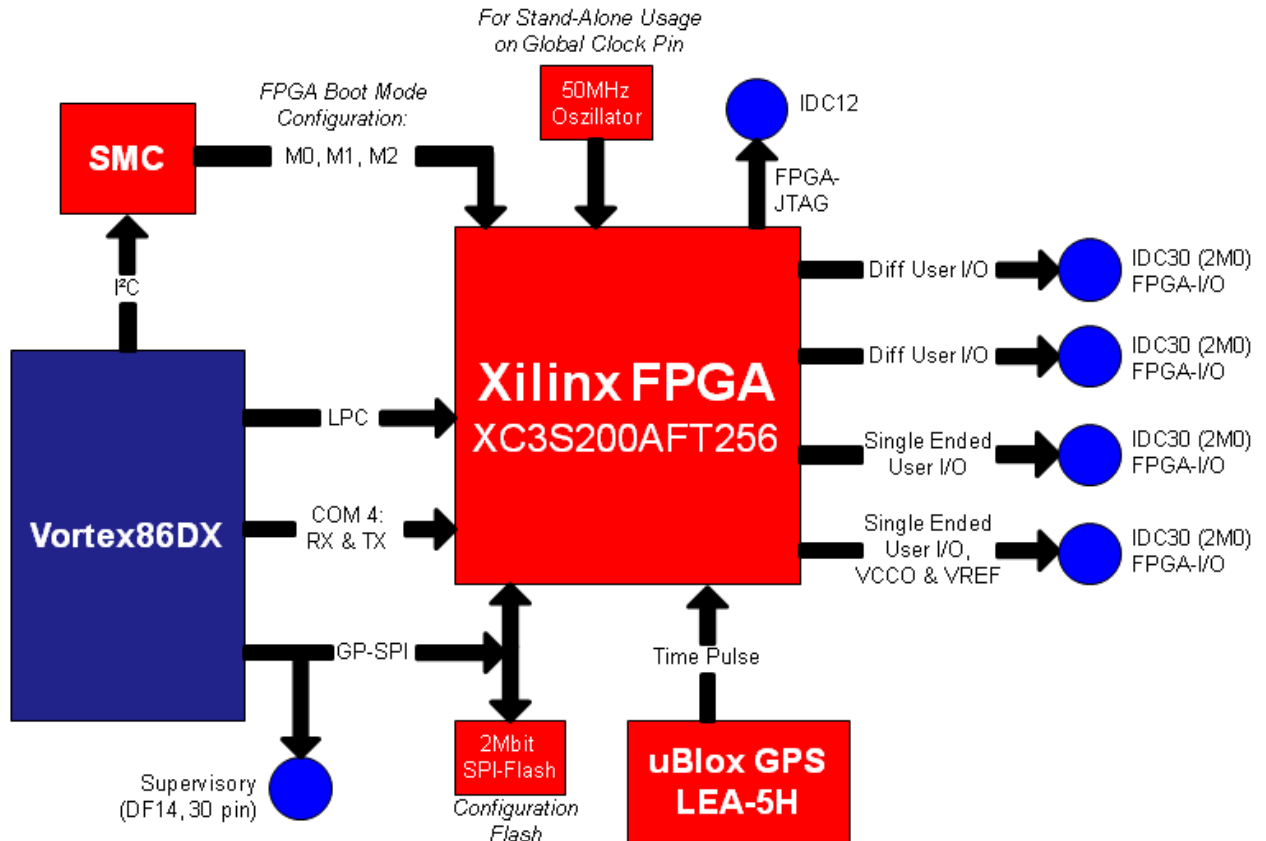
## 1.2 Introduction

The Cool LiteRunner-86DX is a PC/104 board with DMP's Vortex86DX single chip solution, a Xilinx Spartan-3 200A FPGA and a GPS module on board. The FPGA can be used freely by the customer to implement needed functions.

### Features of FPGA XC3S200A on Cool LiteRunner-86DX

System Gates / Equivalent Logic Cells:	200K / 4,032
CLB (Combined Logic Block) Array:	
• Rows / Columns:	32 / 16
• Total CLBs:	448
• Total Slices (1 CLB = 4 Slices):	1,792
Distributed RAM:	28K
Block RAM Bits:	288K
Dedicated Multipliers:	16
DCMs (Digital Clock Manager):	4
Single Ended User I/Os on CLR-86DX:	40 pins
Differential User I/Os on CLR-86DX:	40 pins (Can also be used as Single Ended I/O)
User Global Clocks on CLR-86DX:	12 pins (Can also be used as Differential or Single Ended I/O)

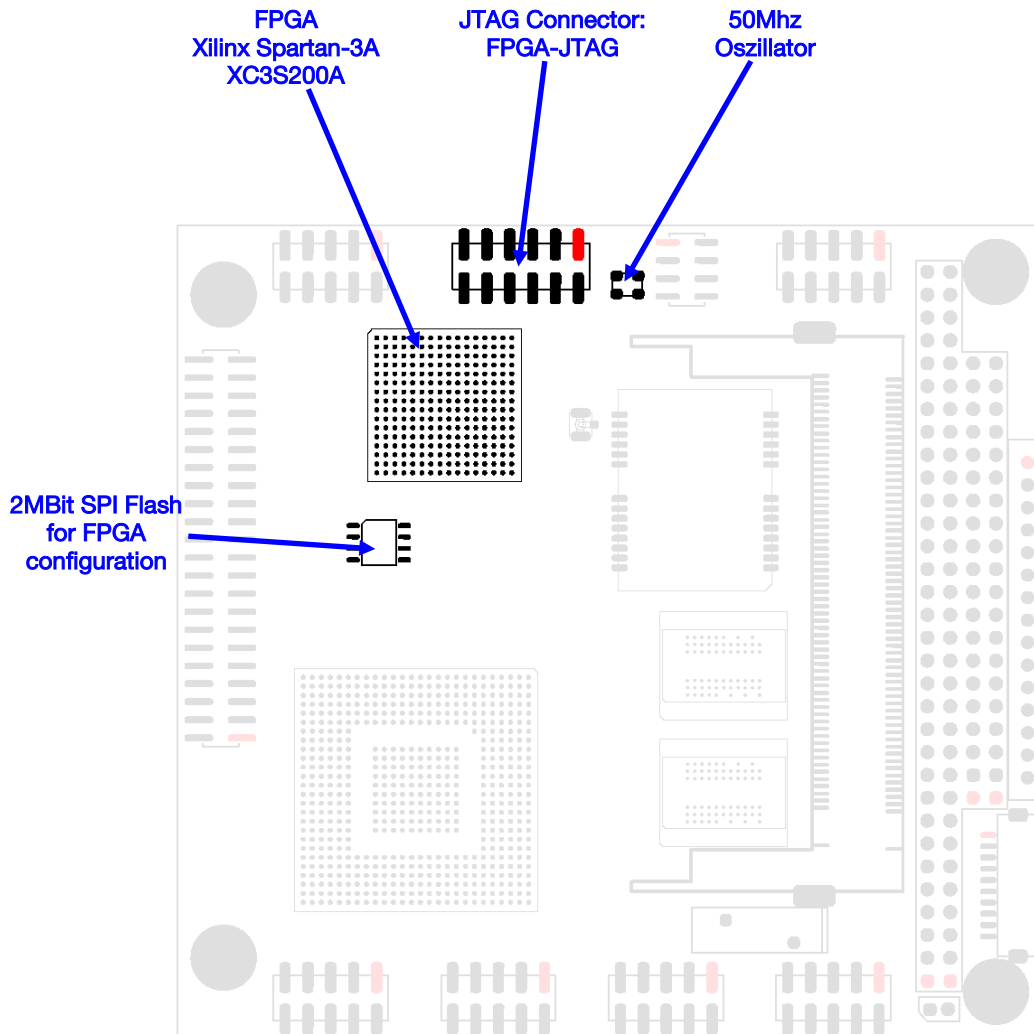
### Block diagram: FPGA on Cool LiteRunner-86DX



## 2 Getting Started

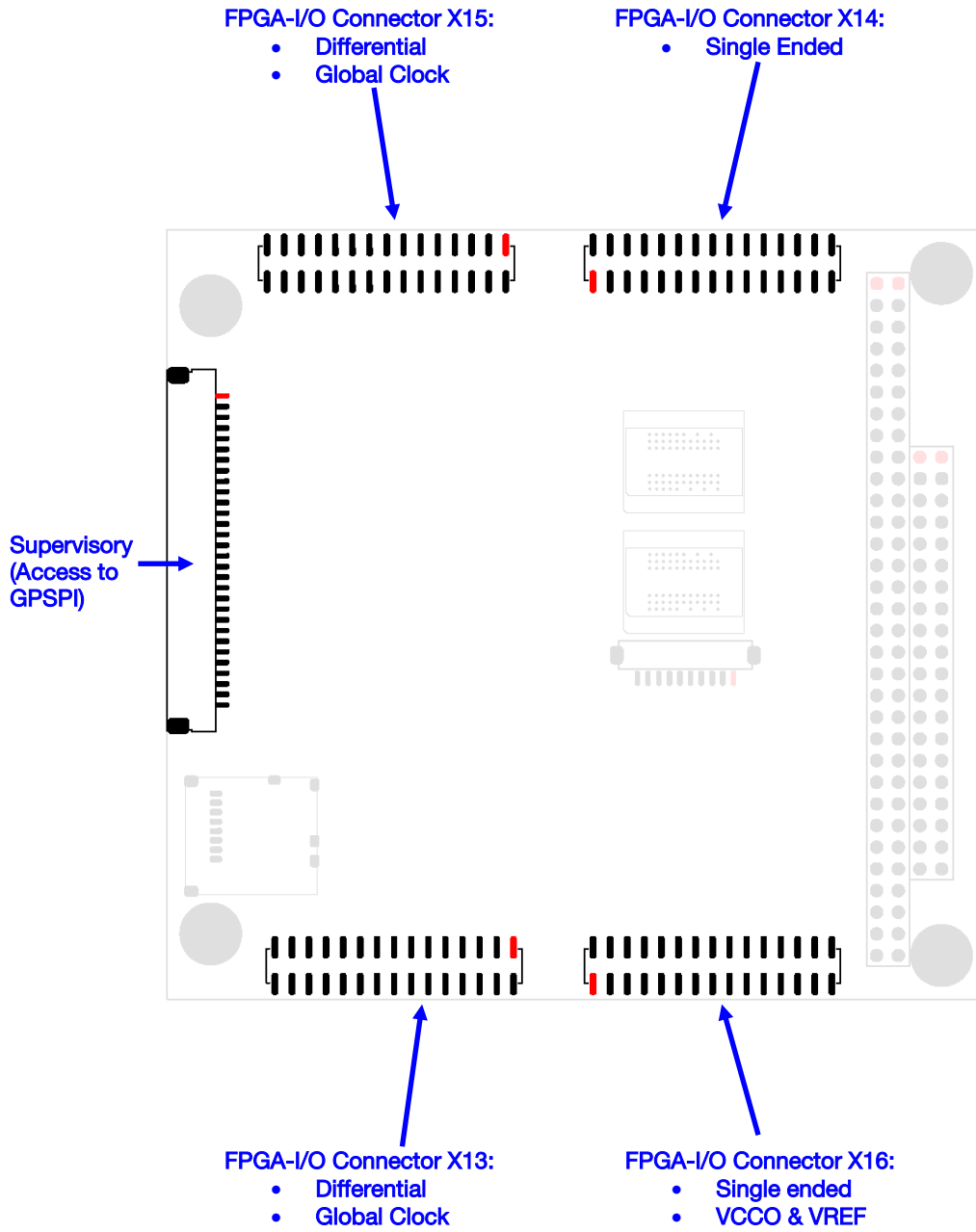
### 2.1 FPGA Relevant Locations

Top



The connectors' pin 1 is marked **RED**

Bottom



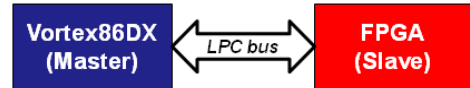
The connectors' pin 1 is marked RED

## 3 Detailed Hardware Description

### 3.1 Vortex86DX

The DMP Vortex86DX SoC on the Cool LiteRunner-86DX is physically connected via LPC bus, COM4 (only RX and TX) and the GP-SPI bus to the Xilinx FPGA. These different busses are used for different tasks:

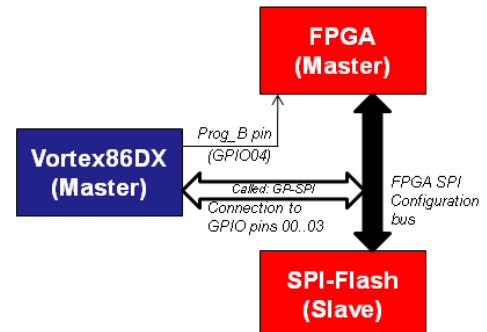
- The LPC (Low Pin Count) bus is some kind of serial ISA bus with a frequency of 33MHz. It can be used for communication between FPGA and Vortex86DX. First a LPC slave has to be designed into the FPGA on the physical LPC pins. The LPC is a master-slave bus, so the slave only sends data to the master on demand. It is accessible under Linux console e.g. with *inb* and *outb*. For LPC Specification please see in appendix B.1 [11].



- RX and TX of COM4 (LVTTTL UART) can also be used for communication between FPGA and Vortex86DX. The FPGA-UART has to be designed on the Physical pins. The Vortex86DX-UART is accessible under Linux with *8250\_pci* module and device */dev/ttyS3*. In opposition to the LPC bus both parts of the UART bus have equal rights. Whenever the FPGA-UART has data to send available on they will be send out directly. To use COM4, make sure the device is activated in the BIOS: **Chipset → Southbridge Configuration → Serial/Parallel Port Configuration**.



- The GP-SPI bus connects the Vortex86DX GPIO port 0 bits 0-3 to the SPI bus between FPGA and SPI-Flash. With GPIO port 0 bit 4 (PROG\_B) the bus masters can be switched:
  - PROG\_B pulled to ground, the Vortex86DX can program a new configuration into the flash.
  - Releasing PROG\_B (GPIO04 to input) and setting GPIO00-03 to input, the FPGA will read out the new configuration from the flash.
  - During board startup the PROG\_B pin should be driven low. Otherwise the FPGA could keep the Vortex from booting. The reason for this is a communication problem on the LPC bus if the FPGA has no proper LPC slave implemented.



To use GP-SPI as flash programming interface please use the V86DX\_GPSPI tool.

For further information regarding the DMP Vortex86DX SoC, please refer to the datasheet of the Vortex86DX (see appendix B.1 [1]).

### 3.2 FPGA (Field Programmable Gate Array)

The Cool LiteRunner-86DX has a FPGA freely useable for I/O extension by the customer. It is a Xilinx Spartan-3A FPGA with 200K Gates. The programming software ("ISE WebPack", see appendix B.1 [9]) is freeware and can be downloaded from the Xilinx home page.

On hardware side the FPGA is physically connected to the LPC bus and the COM4 of the Vortex86DX. By implementing a LPC-slave or UART device into the FPGA a data exchange can take place between FPGA and Vortex86DX.

The FPGA can boot from JTAG or SPI-Flash. The boot mode is SMC controlled and can be changed with the LEMT tool.

For using JTAG, a Xilinx Platform-Cable (USB or LPT) is needed.

The SPI-Flash can be programmed externally over the GP-SPI pins on the Supervisory (e.g. with the Xilinx Platform-Cable) or internally from Vortex86DX over GP-SPI (uses GPIO00 ... 04) with the special flash tool V86DX\_GPSPI (downloadable on the LiPPERT homepage).

Possible I/O Standards of Spartan-3A FPGAs:

Single-Ended Standard	V <sub>cco</sub>	Class	Spec	Use / Sponsor	Input Buffer	Output Buffer	Spartan-3A FPGAs
<b>LVC MOS</b> ( <i>Low Voltage CMOS</i> )	1.2V	-	JESD8C	General purpose	CMOS	Push-Pull	up to 6 mA
	1.5V	-					up to 12 mA
	1.8V	-					up to 16 mA
	2.5V	-					up to 24 mA
	3.3V	-					up to 24 mA
<b>LV TTL</b> ( <i>Low Voltage TTL</i> )	3.3V	-	JESD8C	General purpose 3.3V	LV TTL	Push-Pull	up to 24 mA
<b>PCI 33 / 66</b> ( <i>Peripheral Component Interconnect</i> )	3.0V	-	PCI SIG	PCI bus	LV TTL	Push-Pull	√
	3.3V	-					√
<b>SSTL</b> ( <i>Stub Series Terminated Logic</i> )	1.8V	I, II	JC42.3	SRAM / SDRAM bus; Hitachi and IBM; two classes	V <sub>REF</sub> -based	Push-Pull	√
	2.5V	I, II	JESD8-9				√
	3.3V	I, II	JESD8-8				√
<b>HSTL</b> ( <i>High Speed Transceiver Logic</i> )	1.5V	I, II	JESD8-6	Hitachi SRAM; IBM; three of four classes supported	V <sub>REF</sub> -based	Push-Pull	√
	1.8V	I, II, III					√
<b>GTL</b> ( <i>Gunning Transceiver Logic</i> )	-	-	JESD8-3	High-speed bus, backplane; Xerox	V <sub>REF</sub> -based	Open Drain	
	-	Plus					Intel Pentium Pro

Differential Standard	V <sub>CCO</sub>	Spec	Use / Sponsor	Input Buffer	Output Buffer	Spartan-3A FPGAs
<b>LVDS</b> ( <i>Low Voltage Differential Signaling</i> )	2.5V	ANSI/TIA/EIA-644-A	High-speed interface, back-plane, video; Nation, TI	Diff. Pair	Diff. Pair	√
	3.3V					√
<b>BLVDS</b> ( <i>Bus LVDS</i> )	2.5V	ANSI/TIA/EIA-644-A	Multipoint LVDS	Diff. Pair	Diff. Pair	√
<b>MINI_LVDS</b> ( <i>mini-LVDS</i> )	2.5V	TI	Flat panel displays	Diff. Pair	Diff. Pair	√
	3.3V					√
<b>LVPECL</b> ( <i>Low Voltage Positive ECL</i> )	2.5V	FreeScale Semiconductor (Formerly Motorola)	High-speed clocks	Diff. Pair	Diff. Pair	√
	3.3V					√
<b>RSDS</b> ( <i>Reduced Swing Differential Signaling</i> )	2.5V	National Semiconductors	Flat panel displays	Diff. Pair	Diff. Pair	√
	3.3V					√
<b>TMDS</b> ( <i>Transition Minimized Differential Signaling</i> )	2.5V	Digital Display Working Group	Silicon Image; DVI / HDMI	Diff. Pair	Diff. Pair	√
	3.3V					√
<b>PPDS</b> ( <i>Point-to-Point Differential Signaling</i> )	2.5V	National Semiconductors	LCDs	Diff. Pair	Diff. Pair	√
	3.3V					√
<b>LDT</b> ( <i>Lightning Data Transport (HyperTransport™)</i> )	2.5V	HyperTransport Spec v3.0	Bidirectional serial / parallel high-bandwidth, low latency computer bus; HyperTransport Consortium	Diff. Pair	Diff. Pair	
<b>LVDS EXT</b> ( <i>LVDS Extended</i> )	2.5V	Extension of LVDS	Higher drive requirements	Diff. Pair	Diff. Pair	
<b>DIFF_SSTL</b>	-			Diff. Pair	Diff. Pair	√
<b>DIFF_HSTL</b>	-			Diff. Pair	Diff. Pair	√
<b>DIFF_TERM</b>	-			Diff. Pair	Diff. Pair	√

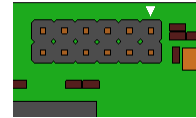
For more information please have a look in the Xilinx FPGA datasheets.

### 3.3 JTAG-FPGA

The JTAG port can be found between COM1 and RS232/485 Termination pin header. It can be used to program the FPGA. Therefore the FPGA boot mode has to be switched to JTAG in the LEMT tool.

Connector type IDC12 pin header 2.54 mm  
Matching connector: IDC12 pin header 2.54 mm, female  
 e.g.: Xilinx Platform Cable USB II

Pin	Signal	Pin	Signal
1	+5.0 V	2	+3.3 V
3	GND	4	GND
5	V86DX_TCK	6	FPGA_TCK
7	V86DX_TDO	8	FPGA_TDO
9	V86DX_TDI	10	FPGA_TDI
11	V86DX_TMS	12	FPGA_TMS

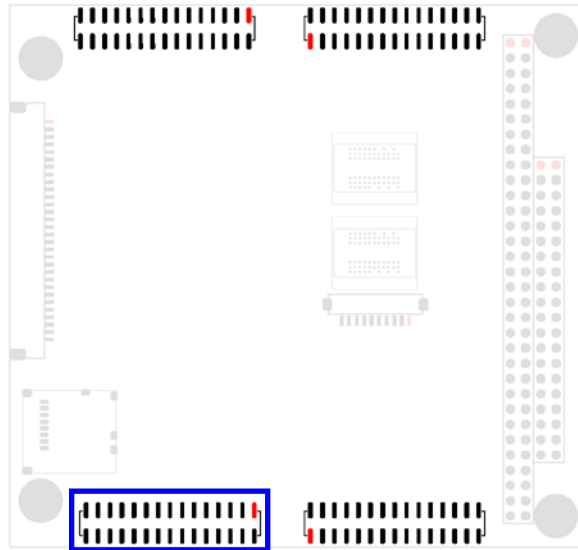


X19

### 3.4 FPGA-I/O Connectors

The I/Os are routed directly to four IDC30 (2mm) connectors. That offers the possibility of a flexible and low-cost Board-to-board or board-to-wire connection. Two connectors are organized as differential pairs and “Global Clock” usage pins. The other two are single ended organized. The FPGA balls are marked by bank: **BANK0**, **BANK1**, **BANK2** and **BANK3**.

Differential signal and “Global Clock” connector 1 (X13)



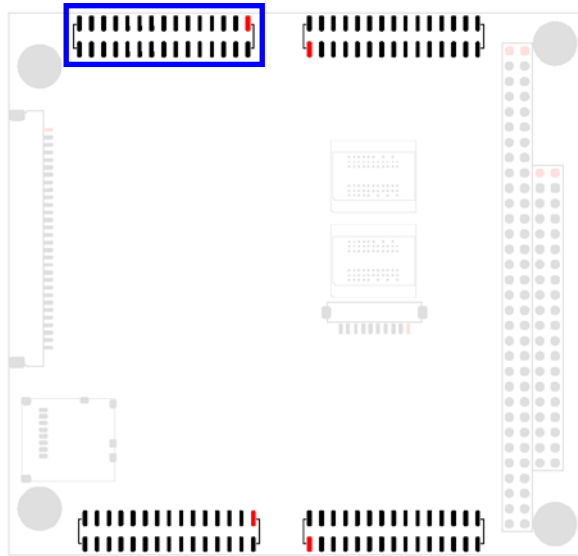
Connector type: IDC30 pin header 2.0 mm  
 Matching connector: IDC30 pin header 2.0 mm, female

Signal name	Wire length [μm]	FPGA ball		FPGA ball	Wire length [μm]	Signal name
3.3 V			(1) (2)			3.3 V
FPGA_IO_DIFF0_P	16526	D13	(3) (4)	C13	16520	FPGA_IO_DIFF0_N
FPGA_IO_DIFF1_P	16834	C12	(5) (6)	D11	16837	FPGA_IO_DIFF1_N
FPGA_IO_DIFF2_P	12806	A14	(7) (8)	A13	12808	FPGA_IO_DIFF2_N
FPGA_IO_DIFF3_P	13174	B12	(9) (10)	A12	13180	FPGA_IO_DIFF3_N
FPGA_IO_DIFF4_P	14203	C11	(11) (12)	A11	14201	FPGA_IO_DIFF4_N
FPGA_IO_DIFF5_P	13881	B10	(13) (14)	A10	13882	FPGA_IO_DIFF5_N
FPGA_IO_GCLK_DIFF6_P	17597	C8	(15) (16)	D8	17587	FPGA_IO_GCLK_DIFF6_N
FPGA_IO_GCLK_DIFF7_P	18273	A8	(17) (18)	B8	18273	FPGA_IO_GCLK_DIFF7_N
FPGA_IO_DIFF8_P	19731	A6	(19) (20)	B6	19731	FPGA_IO_DIFF8_N
FPGA_IO_DIFF9_P	23603	D7	(21) (22)	C6	23609	FPGA_IO_DIFF9_N
FPGA_IO_DIFF10_P	21349	A5	(23) (24)	C5	21352	FPGA_IO_DIFF10_N
FPGA_IO_DIFF11_P	21253	A4	(25) (26)	B4	21246	FPGA_IO_DIFF11_N
FPGA_IO_DIFF12_P	22104	A3	(27) (28)	B3	22098	FPGA_IO_DIFF12_N
GND			(29) (30)			GND

Green Marked: Global Clock Pins

0.5 A is the maximum current for that pin

Differential signal and “Global Clock” connector 2 (X15)

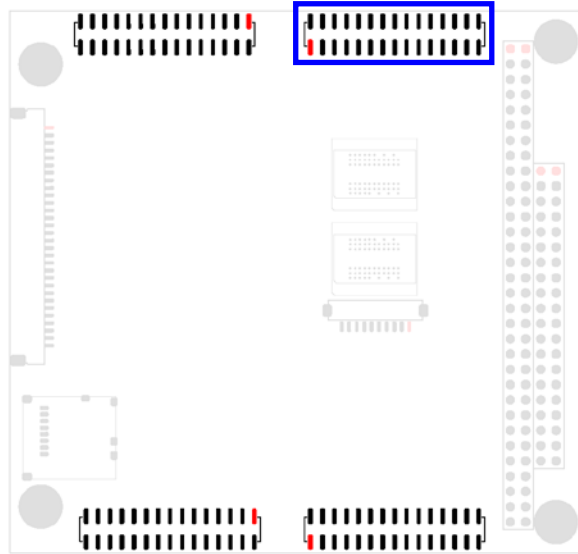


Connector type: IDC30 pin header 2.0 mm  
 Matching connector: IDC30 pin header 2.0 mm, female

Signal name	Wire length [µm]	FPGA ball		FPGA ball	Wire length [µm]	Signal name
3.3 V			(1) (2)			3.3 V
FPGA_IO_DIFF13_P	125971	T4	(3) (4)	R5	125972	FPGA_IO_DIFF13_N
FPGA_IO_DIFF14_P	126316	T5	(5) (6)	T6	126318	FPGA_IO_DIFF14_N
FPGA_IO_DIFF15_P	129232	N7	(7) (8)	P6	129228	FPGA_IO_DIFF15_N
FPGA_IO_DIFF16_P	131179	P7	(9) (10)	N8	131177	FPGA_IO_DIFF16_N
FPGA_IO_GCLK_DIFF17_P	161290	R7	(11) (12)	T7	161286	FPGA_IO_GCLK_DIFF17_N
FPGA_IO_GCLK_DIFF18_P	152166	P8	(13) (14)	T8	152171	FPGA_IO_GCLK_DIFF18_N
FPGA_IO_GCLK_DIFF19_P	133399	N9	(15) (16)	P9	133399	FPGA_IO_GCLK_DIFF19_N
FPGA_IO_GCLK_DIFF20_P	137763	R9	(17) (18)	T9	137765	FPGA_IO_GCLK_DIFF20_N
FPGA_IO_DIFF21_P	121227	N10	(19) (20)	M10	121222	FPGA_IO_DIFF21_N
FPGA_IO_DIFF22_P	114974	P11	(21) (22)	N11	114975	FPGA_IO_DIFF22_N
FPGA_IO_DIFF23_P	107740	T13	(23) (24)	R13	107737	FPGA_IO_DIFF23_N
FPGA_IO_DIFF24_P	103095	N12	(25) (26)	P13	103092	FPGA_IO_DIFF24_N
FPGA_IO_DIFF25_P	97597	N13	(27) (28)	N14	97025	FPGA_IO_DIFF25_N
GND			(29) (30)			GND

Green marked: Global Clock Pins; Blue marked: BANK1

Single-Ended signal connector (X14)

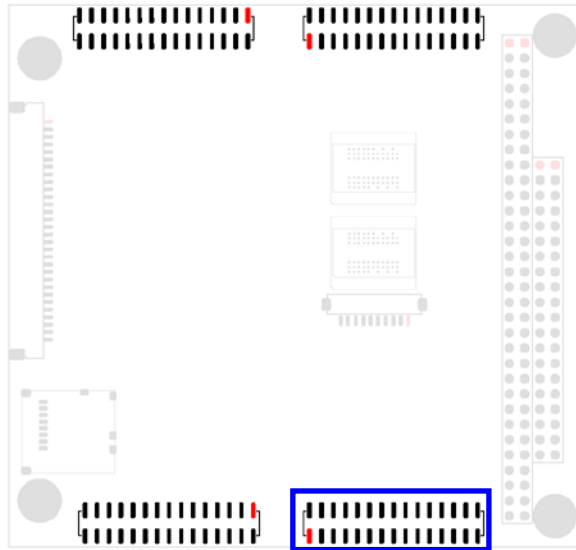


Connector type: IDC30 pin header 2.0 mm  
 Matching connector: IDC30 pin header 2.0 mm, female

Signal name	Wire length [μm]	FPGA ball		FPGA ball	Wire length [μm]	Signal name
3.3 V			(1) (2)			3.3 V
FPGA_IO_SE14	161126	G13	(3) (4)	F13	155568	FPGA_IO_SE15
FPGA_IO_SE16	149225	R15	(5) (6)	P15	147948	FPGA_IO_SE17
FPGA_IO_SE18	150483	P16	(7) (8)	N16	120820	FPGA_IO_SE19
FPGA_IO_SE20	120673	L13	(9) (10)	K13	121877	FPGA_IO_SE21
FPGA_IO_SE22	120935	M15	(11) (12)	M16	116342	FPGA_IO_SE23
FPGA_IO_SE24	118973	L14	(13) (14)	L16	168145	FPGA_IO_SE25
FPGA_IO_SE26	171732	J12	(15) (16)	J13	171348	FPGA_IO_SE27
FPGA_IO_SE28	172060	K15	(17) (18)	K14	176586	FPGA_IO_SE29
FPGA_IO_SE30	164900	K16	(19) (20)	J16	170639	FPGA_IO_SE31
FPGA_IO_SE32	170380	J14	(21) (22)	H14	176179	FPGA_IO_SE33
FPGA_IO_SE34	174428	H15	(23) (24)	H16	173303	FPGA_IO_SE35
FPGA_IO_SE36	171769	G16	(25) (26)	F16	175862	FPGA_IO_SE37
FPGA_IO_SE38	180662	H13	(27) (28)	G14	179895	FPGA_IO_SE39
GND			(29) (30)			GND

· 0.5 A is the maximum current for that pin

Single-Ended signal, VCCO and VREF connector (X16)



Connector type: IDC30 pin header 2.0 mm  
 Matching connector: IDC30 pin header 2.0 mm, female

Signal name	Wire length [µm]	FPGA ball		FPGA ball	Wire length [µm]	Signal name
3.3 V			(1) (2)			3.3 V
3.3 V			(3) (4)			VREF0 (VREF for bank 0)
3.3 V			(5) (6)			VCCO0 (VCCO for bank 0)
3.3 V			(7) (8)			VREF1 (VREF for bank 1)
3.3 V			(9) (10)			VCCO1 (VCCO for bank 1)
3.3 V			(11) (12)			VREF2 (VREF for bank 2)
3.3 V			(13) (14)			VCCO2 (VCCO for bank 2)
FPGA_IO_SE0	51783	A7	(15) (16)	C7	46403	FPGA_IO_SE1
FPGA_IO_SE2	38264	C16	(17) (18)	C15	35383	FPGA_IO_SE3
FPGA_IO_SE4	44760	E13	(19) (20)	D14	38504	FPGA_IO_SE5
FPGA_IO_SE6	42789	D16	(21) (22)	C15	39270	FPGA_IO_SE7
FPGA_IO_SE8	46925	E14	(23) (24)	T10	61253	FPGA_IO_SE9
FPGA_IO_SE10	60273	P12	(25) (26)	F14	44884	FPGA_IO_SE11
FPGA_IO_SE12	49748	E16	(27) (28)	F15	46274	FPGA_IO_SE13
GND			(29) (30)			GND



**Note:** The I/O bank voltage of bank 3 is fix on 3.3V, but voltages of I/O banks 0, 1 and 2 have to be connected first:

For 3.3V usage simply put 2.0mm jumpers onto pins 5-6 (VCCO for bank 0), 9-10 (VCCO for bank 1) and 13-14 (VCCO for bank 2). If VREF of 3.3V is needed just use jumpers on pins 3-4 (VREF for bank 0), 7-8 (VREF for bank 1) and 11-12 (VREF for bank 2).

Other voltages for VREF and VCCO have to be generated externally and connected to the respective pins.

0.5 A is the maximum current for that pin

### 3.5 LPC bus

LPC runs with 33MHz (like PCI) and can be used to exchange data between Vortex86DX and FPGA. To use it first a LPC slave has to be implemented into the FPGA onto the physical pins.

Signal	FPGA ball	Comment
LAD0	C2	<i>Set bidirectional in FPGA designs!</i>
LAD1	C1	<i>Set bidirectional in FPGA designs!</i>
LAD2	D4	<i>Set bidirectional in FPGA designs!</i>
LAD3	D3	<i>Set bidirectional in FPGA designs!</i>
SERIRQ	E1	<i>Set bidirectional in FPGA designs!</i>
LFRAME#	D4	<i>Set bidirectional in FPGA designs!</i>
LDRQ	E3	<i>Set bidirectional in FPGA designs!</i>
LPC_CLK	C10	<i>33MHz, GLCK4, set input in FPGA!</i>
LPC_RST#	E2	<i>Set input in FPGA designs!</i>

### 3.6 COM4

The COM4 interface is a LVTTTL (low voltage TTL level = 3.3V) UART with only RX and TX line. The transfer rate can be up to 115.2 kbps in standard mode and up to 750 kbps in high-speed mode. To use COM4 with the FPGA first a UART slave has to be implemented onto the physical pins.

Signal	FPGA ball	Comment
V86DX_COM4_SIN	K4	<i>TX of FPGA</i>
V86DX_COM4_SOUT	L3	<i>RX of FPGA</i>

### 3.7 Onboard clocks

On the CLR-86DX board there are some clocks lines routed to “global clock” pins of the FPGA. These pins can be used on purpose.

Signal	Frequency	FPGA ball	Comment
LPC_CLK	<b>33.0 MHz</b>	C10	<i>GCLK4, can optional be set to V86DX_CLKOUT</i>
FPGA_50MHZ	<b>50.0 MHz</b>	D9	<i>GCLK5</i>
SUS_CLK	<b>32.768 KHz</b>	C9	<i>GCLK6, Real Time Clock</i>
V86DX_CLKOUT	<b>24.0 MHz</b>	A9	<i>GCLK7, can optional be set to 25.0 MHz</i>

### 3.8 GPS – Global Positioning System

On the Cool LiteRunner-86DX there is a GPS module integrated. In case the module is in reach of enough satellites to calculate its position it generates every second a pulse of 100 milliseconds length on the TimePulse pin. It can be used to synchronize with the GPS or to detect GPS satellite connection.

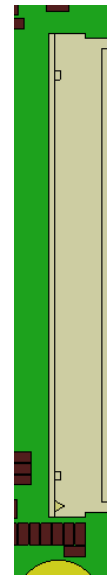
Signal	FPGA ball	Comment
GPS_TIMEPULSE	F3	100 ms pulse every 1 s

### 3.9 Supervisory

The Cool LiteRunner-86DX provides access to the GP-SPI (GPIO based SPI) bus on the Supervisory connector X18. It is located on the bottom side of the board next to the MicroSD slot. The GP-SPI bus connects the FPGA with its SPI-Flash and the Vortex86DX on GPIO00...04.

Connector type DF14 30 pin header 1.25 mm, single row  
Matching connector Hirose DF14-30S-1.25C, Part number 538-0012-3 00

Pin	Signal	Pin	Signal
1	5 V	16	GPIO15
2	3.3 V	17	GPIO16
3	GPIO20	18	GPIO17
4	GPIO21	19	ESPI_CS#
5	GPIO22	20	ESPI_DI
6	GPIO23	21	ESPI_DO
7	GPIO24	22	ESPI_CLK
8	GPIO25	23	I2C_SCL
9	GPIO26	24	I2C_SDA
10	GPIO27	25	GPIO00_CS#
11	GPIO18	26	GPIO01_SCK
12	GPIO17	27	GPIO02_MISO
13	GPIO12	28	GPIO03_MOSI
14	GPIO13	29	GPIO04_PROG_B
15	GPIO14	30	GND



X18

· 1.0 A is the maximum current for each pin

## 4 Using the Module

### 4.1 LEMT functions for the FPGA

The onboard System Management Controller (SMC) implements several functions. These can be used and manipulated with the LEMT (LiPPERT Enhanced Management Technology) tool. The following parts of the FPGA can be configured:

- FPGA Boot Mode (using M0, M1, M2): JTAG, SPI
- *[FPGA Suspend control]* ← Vortex controlled by default, can be changed to SMC control onboard
- *[FPGA PROG\_B control]* ← Vortex controlled by default, can be changed to SMC control onboard

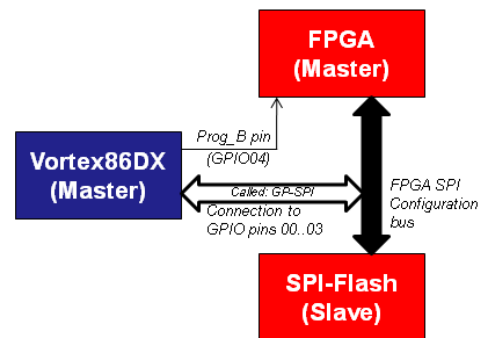


**Note:** LEMT Tools are available for Windows and Linux, LEMT functionality can also be used in applications. Please ask our support for the LEMT software manual and technical manual regarding more details on functionality and how to use it.

### 4.2 GP-SPI Tool

The Vortex86DX is connected to the SPI bus of FPGA and its SPI flash over GPIOs. These GPIOs are called GP-SPI bus (GPIO based SPI bus).

To program the FPGA use the GP-SPI tool. It sets the FPGA to programming mode and writes the configuration into the SPI-Flash. When - after Programming - the FPGA is set back into operation mode, it will read out the configuration from the SPI flash and configure itself.



These are the most important GP-SPI commands:

Application	Command	Options			Comment
./gpspi	id				Read SPI flash ID
	dis				Disable Vortex as GPSPI master: Disable FPGA Programming mode and put FPGA back to operational mode
	be				Bulk Erase: erase whole flash
	etof	0	<size>	<file>	Download SPI flash to file
	wree	0	<file>		Write file to flash



**Note:** The option "0" is an indicator for the addressing mode: flash device, not EEPROM. Do not change!

For FPGA programming you will do well in most cases with this example:

Step	Command	Comment
1.	<code>./gpspi id</code>	check if connection works (should show something different from FF FF FF)
2.	<code>./gpspi be</code>	delete flash contents
3.	<code>./gpspi wree 0 test.bin</code>	write test.bin to SPI flash
4.	<code>./gpspi id</code>	returns a valid ID if programming is finished on chip as well
5.	<code>./gpspi dis</code>	Let FPGA get new configuration

To read back a working configuration from flash back into a file, use this example:

Step	Command	Comment
1.	<code>./gpspi id</code>	check if connection works (should show something different from FF FF FF)
2.	<code>./gpspi etof 0 1FFFFFF test2.bin</code>	delete flash contents
3.	<code>./gpspi dis</code>	Let FPGA get new configuration

### 4.3 IP-Cores

An IP (Intellectual Property) –Core is reusable FPGA software. To implement a special controller, interface or function IP-Cores can be used.

There are companies like Xilinx (see appendix B.1 [8]) offering IP-Cores, which are tested und compliance to the specification. Most of them are commercial. Some small Cores are for free.

Another possibility to get free IP-Cores is the website OpenCores.org (see appendix B.1 [7]). These cores have been written by free developers. In most cases these cores are not tested or verified if they conform to the specification. But it is a good address for help regarding self-developed FPGA software.

## Appendix A, Contact Information

### *Headquarters*

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## Appendix B, Additional Information

### B.1 Additional Reading and Links

#### No. Documents

##### *Vortex86DX*

- [1] DMP Vortex86DX Datasheet and additional material:  
<http://www.dmp.com.tw/tech/vortex86dx/>

##### *FPGA Documents*

- [2] Xilinx Spartan-3A FPGA Family Data Sheet:  
[http://www.xilinx.com/support/documentation/data\\_sheets/ds529.pdf](http://www.xilinx.com/support/documentation/data_sheets/ds529.pdf)
- [3] Xilinx Spartan-3 Generation Configuration User Guide:  
[http://www.xilinx.com/support/documentation/user\\_guides/ug332.pdf](http://www.xilinx.com/support/documentation/user_guides/ug332.pdf)
- [4] Xilinx Spartan-3 Generation FPGA User Guide:  
[http://www.xilinx.com/support/documentation/user\\_guides/ug331.pdf](http://www.xilinx.com/support/documentation/user_guides/ug331.pdf)
- [5] Xilinx Spartan-3A FPGA Application Notes:  
[http://www.xilinx.com/support/documentation/spartan-3a\\_application\\_notes.htm](http://www.xilinx.com/support/documentation/spartan-3a_application_notes.htm)
- [6] Xilinx Spartan-3A FPGA White Papers:  
[http://www.xilinx.com/support/documentation/spartan-3a\\_white\\_papers.htm](http://www.xilinx.com/support/documentation/spartan-3a_white_papers.htm)

##### *FPGA IP-Cores(Intellectual Property)*

- [7] OpenCores.org (free IP-Cores):  
<http://www.opencores.org/>
- [8] Xilinx IP Center:  
<http://www.xilinx.com/ipcenter/>

##### *FPGA Software*

- [9] Xilinx ISE WebPack (free programming tool for Xilinx FPGAs):  
<http://www.xilinx.com/tools/webpack.htm>

##### *GPS*

- [10] uBlox LEA-5H GPS Module Datasheets:  
<http://www.u-blox.com/en/gps-modules/pvt-modules/lea-5h.html>

##### *LPC*

- [11] Low Pin Count (LPC) bus specification:  
<http://www.intel.com/design/chipsets/industry/lpc.htm>

##### *PC104*

- [12] PC/104 Consortium's website:  
<http://www.pc104.org>

## Appendix C, Getting Help

Should you have technical questions that are not covered by the respective manuals, please contact our support department at [support@lippertembedded.com](mailto:support@lippertembedded.com) .

Please allow one working day for an answer!

Technical manuals as well as other literature for all LiPPERT products can be found in the *Products* section of LiPPERT's website [www.lippertembedded.com](http://www.lippertembedded.com). Simply locate the product in question and follow the link to its manual.

### Returning Products for Repair

To return a product to LiPPERT for repair, you need to get a Return Material Authorization (RMA) number first. Please print the RMA Request Form from <http://www.lippertembedded.com/service/repairs.html> fill in the blanks and fax it to +49 621 4321430. We'll return it to you with the RMA number.

**Deliveries without a valid RMA number are returned to sender at his own cost!**

LiPPERT has a written Warranty and Repair Policy, which can be retrieved from <http://www.lippertembedded.com/service/warranty.html>

It describes how defective products are handled and what the related costs are. Please read this document carefully before returning a product.

## Appendix D, Revision History

Filename	Date	Edited by	Change
FME-104-CLR86DX-R0V0	2010-03-09	MS	preliminary draft
FME-104-CLR86DX-R0V1	2010-07-26	MS	Adaption to PCB Rev1V0
FME-104-CLR86DX-R0V2	2010-08-02	MF	minor changes
FME-104-CLR86DX-R0V3	2010-10-12	MS	COM4, available Clocks